

EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|-------|------|---|-----------------------------|------------------|---------|------------------|
| L1 | 26 | ((multi near3 layer\$3) (multi-layer\$3)) near5 monolithic near5 circuit) | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:09 |
| L2 | 13 | 1 and print\$3 | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:09 |
| L3 | 16 | ((multi near3 layer\$3) (multi-layer\$3)) near5 monolithic near5 circuit) | EPO; JPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/22 16:44 |
| L4 | 1 | 3 and print\$3 | EPO; JPO; DERWENT ; IBM_TDB | OR | ON | 2006/07/22 16:44 |
| L6 | 0 | 3 and (laser near5 trim\$3) | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:07 |
| L7 | 0 | 3 and (laser near5 trimm\$3) | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:07 |
| L8 | 2 | 1 and (laser near5 trim\$3) | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:08 |
| L9 | 5155 | (laser near5 trimm\$3) | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:09 |
| L10 | 1909 | 9 and print\$3 | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:09 |
| L11 | 51 | 10 and (monolithic near5 circuit) | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:10 |
| L12 | 26 | 11 and ceramic | US-PGPU B; USPAT; USOCR | OR | ON | 2006/07/22 17:19 |